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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,626	02/23/2006	Sumio Ogawa	Q92356	2062

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
12/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/564,626	OGAWA ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 12/04/2007 has been entered.

2. Claims 1-6, 8, 11-15 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-6, 8,11-15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 8,11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada (U.S. Patent No. 5,982,680).

Regarding claim 1, Wada discloses a semiconductor memory device(Figure 2) which has a redundancy circuit (ABSTRACT), the semiconductor memory device comprising:

a plurality of memory blocks (Figure 2); and

a plurality of redundancy memory blocks (ABSTRACT) provided for each of said plurality of memory blocks,

wherein each of said plurality of memory blocks includes a plurality of segments (Column 1, lines 40-48), said plurality of segments are adjacent to one after another (Figure 2, 20), and

segments having defects among said plurality of segments in a memory block among said plurality of memory blocks (Figure 2) are sequentially allocated to said plurality of redundancy memory blocks and replaced by said allocated redundancy memory blocks (ABSTRACT, Column 1, lines 40-55, lines 65-67, Column 2, lines 1-17).

Regarding claim 2, Wada discloses wherein one each of said plurality of segments includes one or more adjacent memory cell rows or one or more adjacent memory cell columns (Column 2, lines 41-63, Column 3, lines 1-20).

Regarding claim 3, Wada discloses wherein a position of an address bit for selecting said plurality of memory blocks is different from a position of an address bit for selecting said plurality of redundancy memory blocks (Column 2, lines 60-67, Column 3, lines 1-20).

Regarding claim 4, Wada discloses wherein address bits that define said plurality of segments are lower address bits, and address bits for selecting said plurality of redundancy memory blocks include an address bit immediately above said lower address bits (Column 3, lines 1-8, Figure 16).

Regarding claims 5-6, Wada discloses a semiconductor memory device (Figure 2) comprising:

a memory block (Figure 2) having a plurality of segments (Figure 2, 20) , each of said plurality of segments including a plurality of memory cells (ABSTRACTY) ; and

a plurality of redundancy memory blocks (ABSTRACT) which are provided for said memory blocks,

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments (Column 9, lines 19-28) ,

said plurality of segments are allocated to said plurality of redundancy memory blocks ((Column 1, lines 40-48),

a number indicating (Column 9, lines -29) said redundancy memory block allocated to said any segment is given by a remainder generated when an address indicating (Column 3, lines 1-8, lines 16-20) said any segment is divided by a number of said plurality of redundancy memory blocks (Column 6, lines 3-12, Column 9, lines 19-29), and

each of said plurality of segments is replaceable by said redundancy segment of said allocated redundancy memory block if the each of said plurality of segments has a defect (Column 10, lines 55-64).

Regarding claim 8, Wada discloses wherein a first segment and a second segment of said plurality of segments are adjacent to each other (Figure 2, 20), and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks (Figure 2, 20, Column 9, lines 19-29).

Regarding claims 11, 14, Wada discloses wherein each of said plurality of segments is a group of memory cells connected to 2n (n=0, 1, 2 ....) word lines or bit

lines, said word lines are adjacent to one after another when a number of said word lines is plural, and said bit lines are adjacent to one after another when a number of said bit lines is plural (Column 9, lines 30-67, Figures 10-12).

Regarding claims 12, 15, Wada discloses wherein a plurality of lower bits of an address for selecting any of said plurality of segments are input to a decode circuit for selecting said redundancy memory blocks (Column 9, lines 30-67, Column 10, lines 1-37).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827